

MC100LVEL51

3.3V ECL Differential Clock D Flip-Flop

Description

The MC100LVEL51 is a differential clock D flip-flop with reset. The device is functionally equivalent to the EL51 device, but operates from a 3.3 V supply. With propagation delays and output transition times essentially equal to the EL51, the LVEL51 is ideally suited for those applications which require the ultimate in AC performance at 3.3 V V_{CC} .

The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the LVEL51 allow the device to be used as a negative edge triggered flip-flop.

The differential input employs clamp circuitry to maintain stability under open input conditions. When left open, the CLK input will be pulled down to V_{EE} and the \overline{CLK} input will be biased at $V_{CC}/2$.

Features

- 475 ps Propagation Delay
- 2.8 GHz Toggle Frequency
- ESD Protection: >4 kV Human Body Model, >200 V Machine Model
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: $V_{CC} = 3.0\text{ V}$ to 3.8 V with $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0\text{ V}$ with $V_{EE} = -3.0\text{ V}$ to -3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 114 devices
- Pb-Free Packages are Available



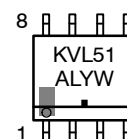
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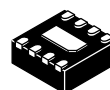
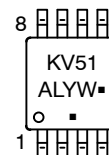
MARKING DIAGRAMS*



SOIC-8
D SUFFIX
CASE 751



TSSOP-8
DT SUFFIX
CASE 948R



DFN8
MN SUFFIX
CASE 506AA



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
M̄ = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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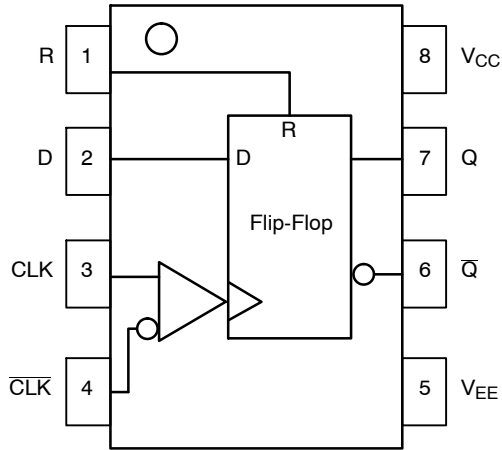


Figure 1. Logic Diagram and Pinout Assignment

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{\text{CLK}}$	ECL Differential Clock Input
Q, $\overline{\text{Q}}$	ECL Differential Output
D	ECL D Input
R	ECL Reset Input
V _{CC}	Positive Supply
V _{EE}	Negative Supply
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

Table 2. TRUTH TABLE

D	R	CLK	Q
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

X = Don't Care

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Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8 to 0	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-8 to 0	V
V _I	PECL Mode Input Voltage	V _{EE} = 0 V	V _I ≤ V _{CC}	6 to 0	V
	NECL Mode Input Voltage	V _{CC} = 0 V	V _I ≥ V _{EE}	-6 to 0	V
I _{out}	Output Current	Continuous		50	mA
		Surge		100	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm	8 SOIC	190	°C/W
		500 lfpm	8 SOIC	130	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	8 SOIC	41 to 44 ± 5%	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm	8 TSSOP	185	°C/W
		500 lfpm	8 TSSOP	140	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	8 TSSOP	41 to 44 ± 5%	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm	DFN8	129	°C/W
		500 lfpm	DFN8	84	°C/W
T _{sol}	Wave Solder	Pb		265	°C
		Pb-Free		265	°C
θ _{JC}	Thermal Resistance (Junction-to-Case)	(Note 1)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

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Table 4. LVPECL DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$; $V_{EE} = 0.0\text{ V}$ (Note 1)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		30	35		30	35		32	37	mA
V_{OH}	Output HIGH Voltage (Note 3)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 3)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 7) $V_{PP} < 500\text{ mV}$ $V_{PP} \geq 500\text{ mV}$	1.2		3.0	1.1		3.0	1.1		3.0	V
		1.4		3.0	1.3		3.0	1.3		3.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others CLK	0.5			0.5			0.5			μA
		-600			-600			-600			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.
- Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.
- V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1 V .

Table 5. LVNECL DC CHARACTERISTICS $V_{CC} = 0.0\text{ V}$; $V_{EE} = -3.3\text{ V}$ (Note 5)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		30	35		30	35		32	37	mA
V_{OH}	Output HIGH Voltage (Note 6)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage (Note 6)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 7) $V_{PP} < 500\text{ mV}$ $V_{PP} \geq 500\text{ mV}$	-2.1		-0.3	-2.2		-0.3	-2.2		-0.3	V
		-1.9		-0.3	-2.0		-0.3	-2.0		-0.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others CLK	0.5			0.5			0.5			μA
		-600			-600			-600			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.
- Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.
- V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1 V .

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Table 6. AC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$; $V_{EE} = 0.0\text{ V}$ or $V_{CC} = 0.0\text{ V}$; $V_{EE} = -3.3\text{ V}$ (Note 8)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{\max}	Maximum Toggle Frequency	2.7			2.8			2.9			GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK R	330 340	465 455	510 540	340 350	475 465	520 550	370 390	530 510	550 590	ps
t_{S}	Setup Time	150	0		150	0		150	0		ps
t_{H}	Hold Time	200	100		200	100		200	100		ps
t_{RR}	Reset Recovery	350	200		350	200		350	200		ps
t_{PW}	Minimum Pulse Width CLK Reset	400 500			400 500			400 500			ps
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 9)	150		1000	150		1000	150		1000	mV
t_{r} t_{f}	Output Rise/Fall Times Q (20% - 80%)	120		320	120		320	120		320	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. V_{EE} can vary $\pm 0.3\text{ V}$.

9. $V_{\text{PP}}(\text{min})$ is minimum input swing for which AC parameters are guaranteed.

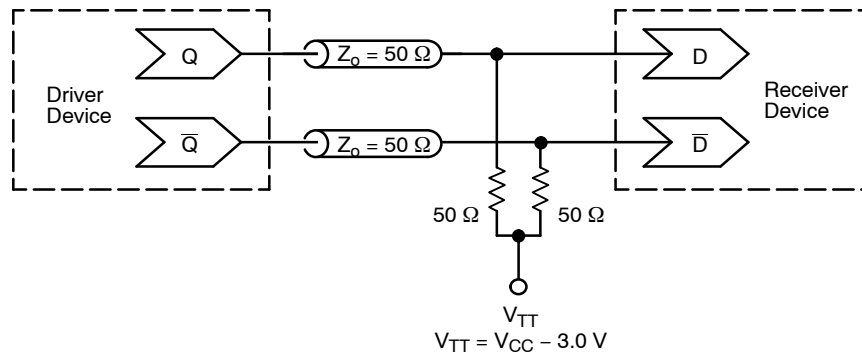


Figure 2. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

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ORDERING INFORMATION

Device	Package	Shipping†
MC100LVEL51D	SOIC-8	98 Units / Rail
MC100LVEL51DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC100LVEL51DR2	SOIC-8	2500 / Tape & Reel
MC100LVEL51DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100LVEL51DT	TSSOP-8	100 Units / Rail
MC100LVEL51DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100LVEL51DTR2	TSSOP-8	2500 / Tape & Reel
MC100LVEL51DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100LVEL51MNR4	DFN8	1000 / Tape & Reel
MC100LVEL51MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

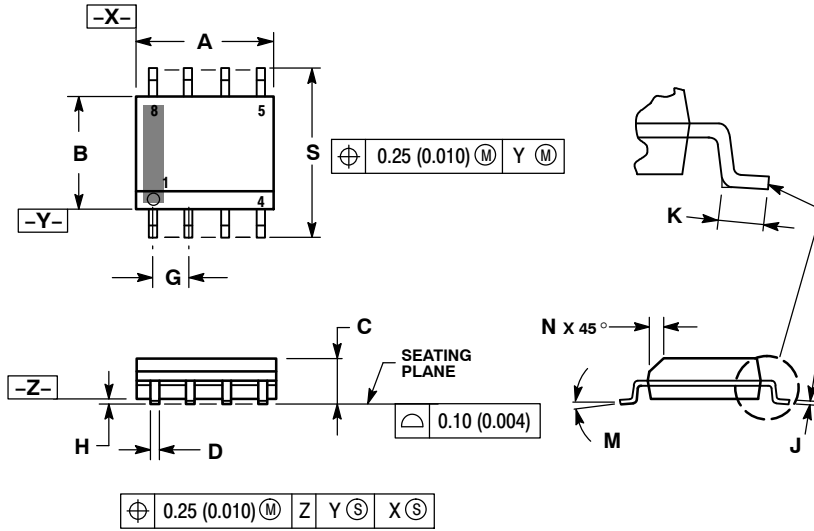
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AJ

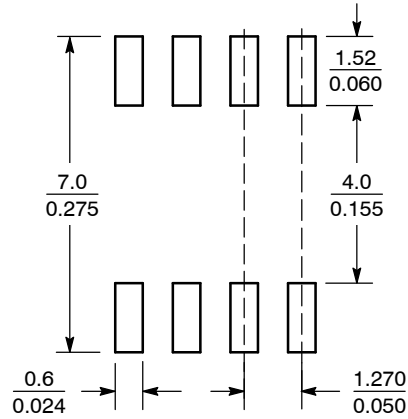


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



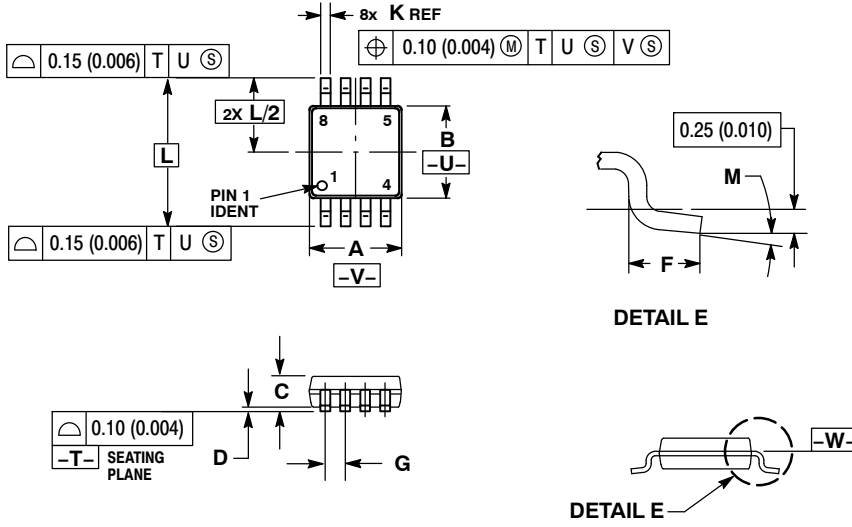
SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

TSSOP-8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R-02
ISSUE A



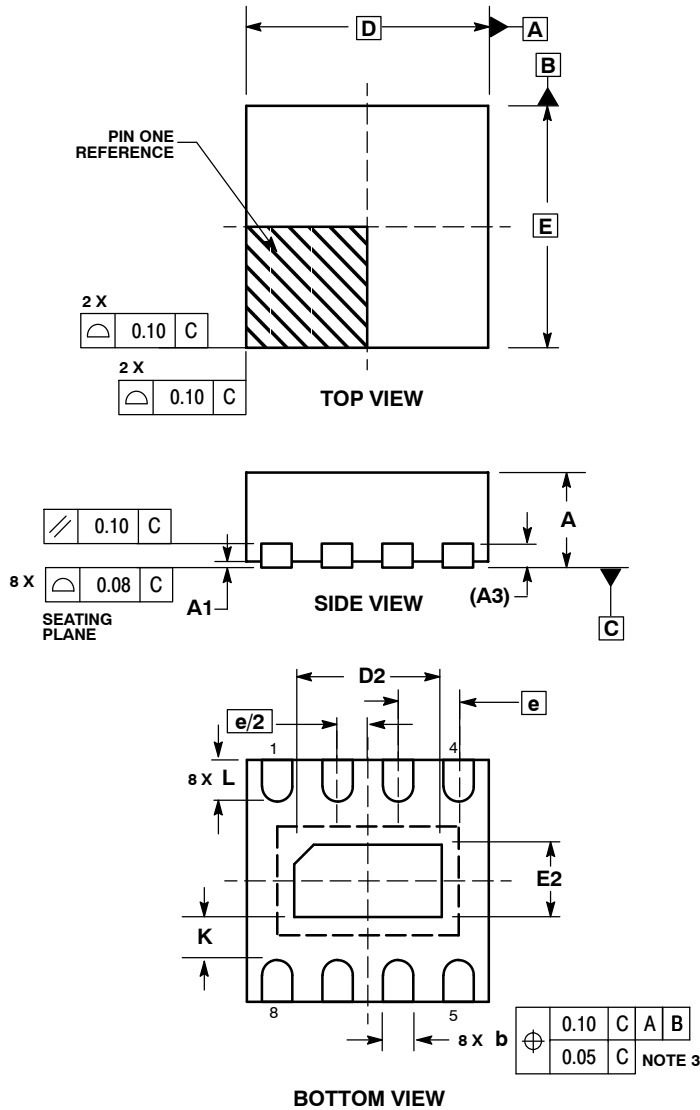
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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PACKAGE DIMENSIONS

DFN8
CASE 506AA-01
ISSUE D



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.20	---
L	0.25	0.35

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